

CLAIMS

What is claimed is:

3 ~~1. A system comprising:~~

4 ~~a processor coupled to memory by a bus, the processor having a processor core~~

5 ~~and a pad ring, the processor core having an independent power supply;~~

6 ~~a voltage regulator providing a plurality of voltages and providing the independent~~
7 ~~power supply;~~

8 ~~a clock signal generator providing a clock signal at a plurality of frequencies;~~

9 ~~a state machine to coordinate voltage and clock frequency to the processor core; and~~

10 ~~an operating system running on the processor, the operating system monitoring an~~
11 ~~application mix executing in the processor to determine a required frequency, and determining a~~
12 ~~minimum voltage at which the processor core can operate at the required frequency, wherein the~~
13 ~~operating system directs the state machine to enter a state in which the required frequency is~~
14 ~~supplied by the clock signal generator and a closest supported voltage equal to or greater than the~~
15 ~~minimum voltage is supplied by the voltage regulator.~~

1 2. The system of claim 1 wherein the voltage regulator provides one of an

2 idle voltage of a peak voltage.

3. The system of claim 1 wherein the voltage regulator can provide one
voltage corresponding to each frequency supported by the clock signal generator.

1 4. A method of reducing power consumption by a processor core and a pad ring
2 comprising the steps of:

3 ~~accepting a measure of processor core performance need of each application~~
4 currently seeking access to the processor core;
5 accumulating each measure of processor core performance need to find total current
6 need:
7 calculating a minimum frequency that will allow the processor core to meet the total
8 current need for the time period:
9 selecting a lowest supported frequency equal to or greater than the minimum
10 frequency to be a required frequency:
11 finding a minimum supported voltage at which the processor core can operate at the
12 required frequency independent of a voltage required by the pad ring;
13 supplying the required frequency and the minimum supported voltage to the
14 processor core; and
15 dynamically changing the required frequency and the minimum supported voltage supplied
16 responsive to a change in the current application mix.

1 5. A method of reducing power consumption by a processor core and a pad ring
2 comprising the steps of:
3 establishing a maximum allowable power consumption;
4 finding a maximum supported frequency which will allow the processor core to
5 remain below the maximum allowable power consumption at the minimum supported voltage;
6 selecting a required frequency to be less than or equal to the maximum supported
7 frequency:
8 finding a minimum supported voltage at which the processor core can operate at the
9 required frequency independent of a voltage required by the pad ring:
10 supplying the required frequency and the minimum supported voltage to the

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11 processor core: and
12 dynamically changing the required frequency and the minimum supported voltage
13 supplied responsive to a change in the current application mix.

14 6. The method of claim 5 wherein a required frequency less than the
15 maximum supported frequency is selected whenever a total processor
16 core performance need of the current application mix can be met by a lower
17 supported frequency

add D5

Add #1
Add B5
Add F1